What is claimed is:

CLAIMS

1. Apparatus for converting a serially received data word to a parallel output data word, said apparatus comprising:

a serial data input interface that receives the serially received data word, and provides a received data word;

a serial-to-parallel mapping circuit that receives said received data word and generates memory write control and write address signals;

a memory device having a first port responsive to said memory write control signals and write address signals for writing said received data word into said memory device, and a second port responsive to memory read control and read address signals for reading data from said memory device; and

output interface circuitry that generates said memory read control and read address signals, and receives output data from said memory device and reorders the bits of said output data to provide a parallel output data word.

2. The apparatus of claim 1, wherein said serial-to-parallel mapping circuit comprises means for partitioning said received data word into a plurality of partitioned received data words and for generating said memory write control signals such that said partitioned received data words are written into said memory device at uniquely associated memory addresses.

3. The apparatus of claim 2, wherein said output interface circuitry comprises an output mapping circuit responsive to said output data and a parallel output interface, wherein

reordering of the bits said output data word by mapping interconnects between an output port of said output mapping circuit and an input port parallel output interface, wherein said parallel output interface also includes a parallel output interface output port that provides the parallel output data word.

4. The apparatus of claim 1, wherein said output interface circuitry comprises an output mapping circuit that reads a word from said memory device, wherein said word read from said memory has an equal number of bits as said serially received data word.

5. The apparatus of claim 1, wherein said serial data interface clocks in said serially received data word at a first rate and said serial-to-parallel mapping circuit clocks data at a second rate having a frequency least eight times faster than said first rate.

6. Apparatus for converting a parallel received data word to a serial data word, said apparatus comprising:

a memory device having a first port responsive to memory write control and write address signals, and a second port responsive to memory read control and read address signals;

a parallel-to-serial mapping circuit that receives the parallel received data word and generates said memory write control and write address signals to write a bit shuffled version of said parallel received data word into said memory device; and

a data output interface that generates said memory read control and read address signals to perform reads from said memory device and receives output data from said memory device to provide the serial data word.

7. The apparatus of claim 6, wherein said memory device comprises a RAM device.

8. A serial-to-parallel/parallel-to-serial conversion engine, comprising:

A) serial-to-parallel conversion path that includes

A1) a serial data input interface that receives a serially received data word, and provides a received data word;

A2) a serial-to-parallel mapping circuit that receives said received data word and generates first memory write control and write address signals;

A3) a first memory device having a first port responsive to said first memory write control signals and write address signals for writing said received data word into said first memory device, and a second port responsive to first memory read control and read address signals for reading data from said first memory device;

A4) output interface circuitry that generates said first memory read control and read address signals, and receives output data from said first memory device and reorders the bits of said output data to provide a parallel output data word;

B) a parallel-to-serial data conversion path that includes

B1) a second memory device having a third port responsive to second memory write control and write address signals, and a fourth port responsive to second memory read control and read address signals;

B2) a parallel-to-serial mapping circuit that receives the parallel received data word and generates said second memory write control and write address signals to write a bit shuffled version of said parallel received data word into said second memory device; and

B3) a data output interface that generates said second memory read control and read address signals to perform reads from said second memory device and receives output data from said second memory device to provide a serial data word.